Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.017”**

****

**.017”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: COLLECTOR**

**Mask Ref: G2**

**APPROVED BY: DK DIE SIZE .017” X .017” DATE: 10/5/22**

**MFG: ZETEX THICKNESS .005” P/N: BC858**

**DG 10.1.2**

#### Rev B, 7/19/02